EE / CprE / SE 491 – sdmay20-10
Power Scraping Module
Week 4 Report
10/14/2019 -10/27/2019
Client: Honeywell FM&T
Faculty Advisor: Gary Tuttle

Team Members/Role:

Jordan Fox — Chief Engineer
Xiangyu Cao — Design Engineer
Andesen Ande — Design Engineer
Ahmed Salem — Test Engineer
Ben Yoko — Test Engineer
Shahzaib Shahid — ***Team Leader***

Weekly Summary

This week we got our schematic reviewed by our faculty advisor and client. After sending the proposed design to our faculty advisor we recieved feedback on how to imrove design and finalized parts of the design that we had questions on. We then had a meeting with our client to get our proposed design approved. Once we informed clients of changes in our design and got them improved we ordered parts. All parts were ordered together and are expected to arrive in two weeks.

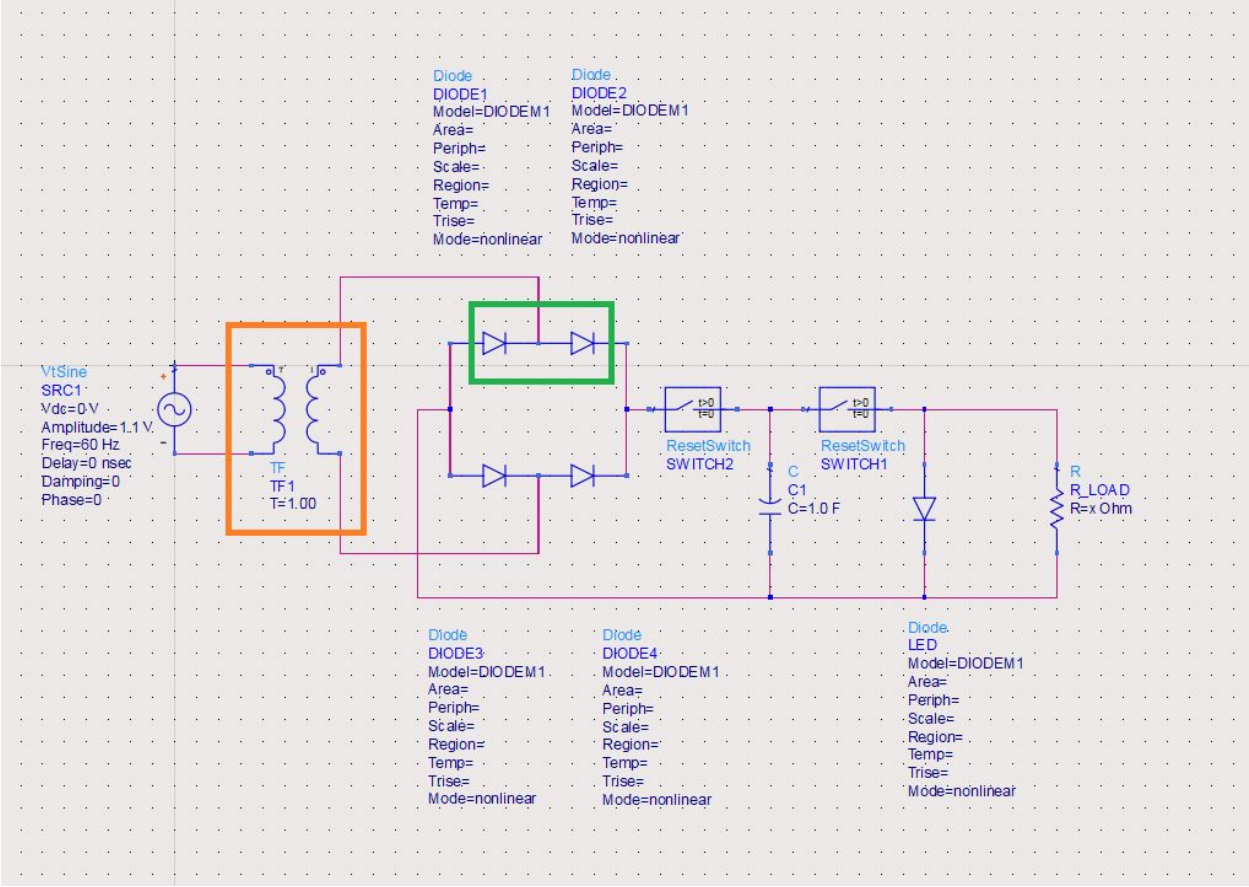
Past Week Accomplishments

Timeline:

TASK NAME	START DATE	END DATE	DURATION* (WORK DAYS)	DAYS COMPLETE*	DAYS REMAINING*	TEAM MEMBER	PERCENT COMPLETE
First Sample Project							
Team Formations & Project Descriptions	8/26	8/31	6	6	0	Shahzaib Shahid	100%
Team Expectation and Setting Roles	9/2	9/7	6	6	0	Andesen Ande	100%
Meeting with Faculty	9/9	9/11	3	3	0	Benjamin Yoko	100%
Design Document Formation	9/12	9/13	2	2	0	Xiangyu Cao	100%
Project Description & Lightening Talk	9/16	9/20	5	5	0	Ahmed Salem	100%
Pre-liminary Design Schematic	9/23	9/27	5	5	0	Jordan Fox	100%
Second Sample Project							
Assigning project	9/30	10/4	5	5	0	Shahzaib Shahid	100%
Search For Parts & meeting with Faculty and Client	10/7	10/11	5	4	1	Andesen Ande	80%
Confirm Budget and Confirm Timeline	10/14	10/16	3	2.25	1	Benjamin Yoko	75%
Meeting with Faculty on design options	10/17	10/18	2	2	0	Xiangyu Cao	100%
Weekly Status Report 4, Design Document Version 2 (near completion), Contact Client	10/21	10/24	4	2.8	1	Ahmed Salem	70%
Build a Schematic & meeting with Faculty on design options	10/25	10/27	3	2.7	0	Jordan Fox	90%
Third Sample Project							
Pre-liminary Design Schematic, Weekly Status Report #3, Design Document Expansion	10/28	11/1	5	3.5	2	Shahzaib Shahid	70%
Look For Parts, Confirm and Discuss Design with Faculty and Client	11/4	11/8	5	3.85	1	Andesen Ande	77%
Discuss Design, Look For more Parts and Confirm Budget,	11/11	11/13	3	2.28	1	Benjamin Yoko	76%
Confirm Timeline and Schedule	11/14	11/15	2	1.6	0	Xiangyu Cao	80%
Weekly Status Report 4, Design Document Version #2 (near completion)	11/18	11/29	12	9	3	Ahmed Salem	75%
Get Parts, Build Prototype on Breadboards, Weekly Status Report #5.	12/2	12/6	5	3	2	Jordan Fox	60%
Fourth Sample Project							
Build Prototype on Breadboards, Design Document V3,	12/9	12/13	5	1.5	4	Shahzaib Shahid	30%
Testing of the Breadboard Prototype, Weekly Status Report 6	12/10	12/14	5	0	5	Andesen Ande	0%
Check For Issues and Testing For Improvements	12/11	12/12	2	0	2	Benjamin Yoko	0%
Design Efficiency Check	12/13	12/15	3	0	3	Xiangyu Cao	0%
Final Prototype Design and Testing. Final Design Document	12/12	12/16	5	0	5	Ahmed Salem	0%
Final Presentation for the Design.	12/13	12/17	5	0	5	Jordan Fox	0%

As part of our design document we were required to create a gantt chart. This chart is a type of formatting for a project schedule. Each task is desribed, given a timeline, it's progress is tracked in terms of days, and assigned to a team member. This chart is the most comprehensive chart we made to track our progress. This is important for our client and faculty advisor to assess if everyone is doing their part and to track how well the process is going. It's also convient to have clarity in what we are doing on a week to week basis with an end goal that we are all aware of.

Design Modification:



- Above is a schematic of our primary design as seen in our last weekly report. After meeting with our faculty advisor we made two changes. The first change we discussed was removing two out of the four diodes in the rectfication stage. Our intention of placing four diodes was to take utilize the entire sinusoid of the input signal. However this came at a cost of a greater voltage drop. We were advised to remove the two diodes (highlighted in green) because the voltage drop was too signficant. The other change was the voltage booster stage (highlighted in orange). We created this stage as a placeholder for a device that could boost AC voltage. Unfortunately, we could not find such a device and so our design has been modified to have the rectification stage (green) as the first stage. This was done because we found a DC-DC voltage booster that meets our design objectives. As a result we are going to convert input signal to DC voltage before amplifying and storing.

Individual Contributions

Name	**Hours this week**	**Hours Cumulative**
Jordan Fox	6.5	25.5
Xiangyu Cao	6.5	25.5
Andesen Ande	7	25.5
Ahmed Salem	6	25
Ben Yoko	7.5	26
Shahzaib Shahid	6.5	25

*Reported times are rough estimates.

Plans for the upcoming week

1. Wait for our parts to arrive and plan protoype-all team members
    a. Decide test objectives, and methods
    b. Divide tasks
2. Complete section 5 in our design document. This section is dedicated to testing. This is an optimal time to plan how we want to protoype and test while waiting for parts.
    a. 5.1 -Jordan
    b. 5.2 -Ahmed
    c. 5.3-Shahzaib
    d. 5.4-Cao
    e. 5.5-Andesen
    f. 5.6-Ben
3. Being preparing for client mid-year presentation-all team members
    a. Find out the requirements of the presentation
    b. Once we get an idea of what is required we will then begin assigning each part of the presentation to each member